

TQELN8122V5

Low Capacitance Array for ESD Protection

● Description

The TQELN8122V5 provides a typical line to line capacitance of 1.1pF and low insertion loss up to 2GHz providing greater signal integrity making it ideally suited for GbE, USB 2.0 applications, such as Digital TVS, DVD players, Computer, set-top boxes and MDDI applications in mobile computing devices.

It has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over voltage caused by Lighting, ESD(electrostatic discharge), CDE (Cable Discharge Events),and EFT (electrical fast transients).

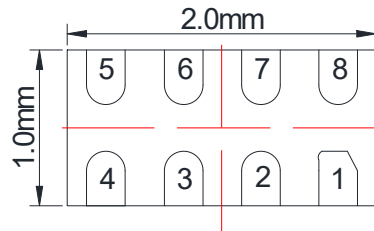
● Feature

- protects eight I/O lines
- Low capacitance: 0.47pF
- Working voltages : 2.5V
- Low leakage current
- Response Time is < 1 ns
- Low capacitance for high-speed interfaces
- No insertion loss to 2.0GHz
- Solid-state silicon avalanche technology
- Meets MSL 1 Requirements
- ROHS compliant
- TECH CHIP technology

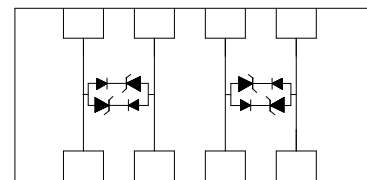
● Protection solution to meet

- IEC61000-4-2 (ESD) $\pm 22\text{kV}$ (air), $\pm 22\text{kV}$ (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)

● PIN configuration



DFN2010-8L



● Applications

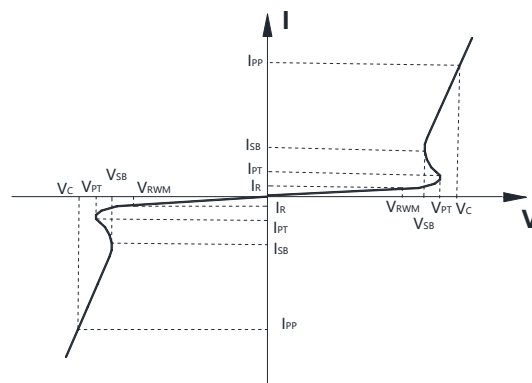
- Digital Visual Interface (DVI)
- 10/100/1000 Ethernet
- USB 1.1/2.0/OTG
- IEEE 1394 Firewire Ports
- Projection TV Monitors and Flat Panel Displays
- Notebook Computers
- Set Top Box
- Projection TV

● Mechanical data

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260°C
- Device meets MSL 1 requirements
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

Electronic Parameter

Symbol	Parameter
V_{RWM}	Working Peak Reverse Voltage
V_{PT}	Punch-Through Voltage@ I_{PT}
V_{SB}	Snap-Back Voltage@ I_{SB}
V_C	Clamping Voltage @ I_{PP}
I_T	Test Current
I_{RM}	Leakage current at V_{RWM}
I_{PP}	Peak pulse current
C_J	Junction Capacitance



● Absolute maximum rating @TA=25°C

Symbol	Parameter	Value	Units
P_{PPP}	Peak Pulse Power (tp=8/20μs waveform)	400	Watts
	ESD Rating per IEC61000-4-2:		
	Contact	+/- 30	KV
	Air	+/- 30	
T_L	Lead Soldering Temperature	260 (10 sec.)	°C
T_J	Operating Temperature Range	-55 ~ 150	°C
T_{STG}	Storage Temperature Range	-55 ~ 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

*Other voltages may be available upon request.

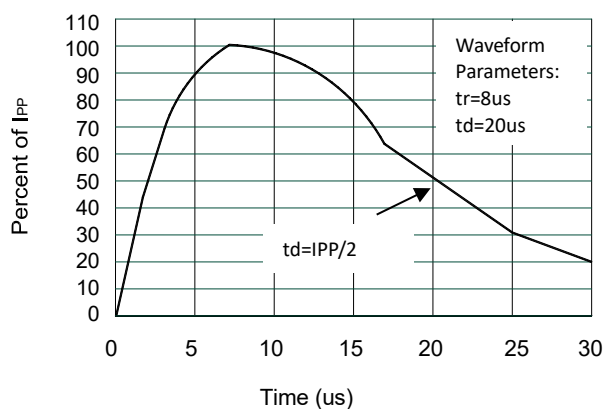
1. Non-repetitive current pulse, per Figure 1.

● Electrical Characteristics @TA=25°C

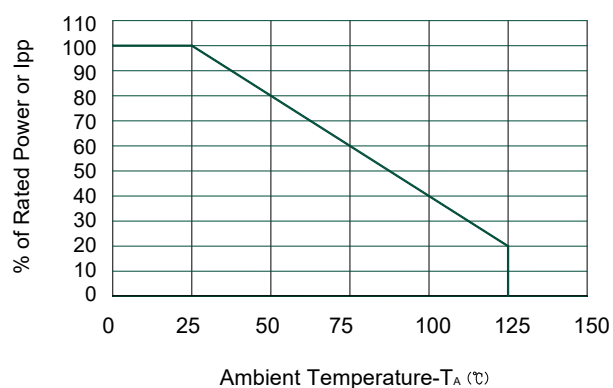
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	between I/O pins			2.5	V
V_{SB}	Snap-Back Voltage	$I_{SB} = 45mA$, between I/O pins	2.8			V
V_{PT}	Punch-Through Voltage	$I_{PT} = 2\mu A$ between I/O pins	3.5			V
I_R	Reverse Leakage Current	$V_{RWM} = 2.5V$, between I/O pins			0.05	μA
V_C	Clamping Voltage between I/O pins	$I_{PP} = 1A$, $t_p = 8/20\mu s$		4.7	5.6	V
		$I_{PP} = 20A$, $t_p = 8/20\mu s$		15.1	22	V
C_J	Junction Capacitance	$V_R = 0V$, $f = 1MHz$, between I/O pins		1.1		pF
C_J	Junction Capacitance	$V_R = 2.5V$, $f = 1MHz$, between I/O pins		0.47	0.9	pF

Junction capacitance is measured in $V_R=0V, F=1MHz$

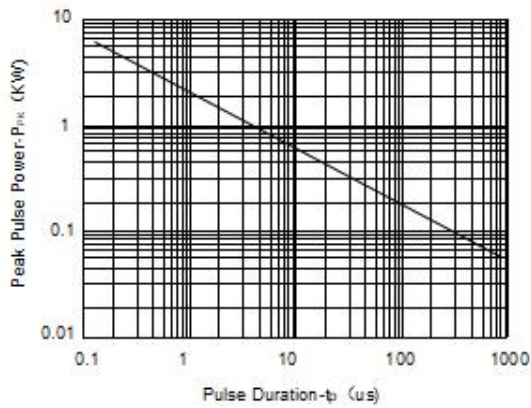
● Typical Performance Characteristics



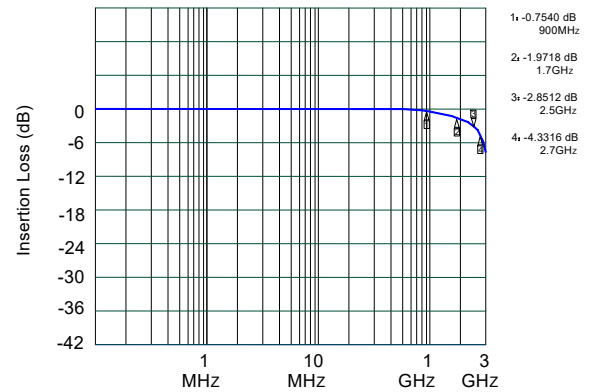
Pulse Waveform



Power Derating Curve



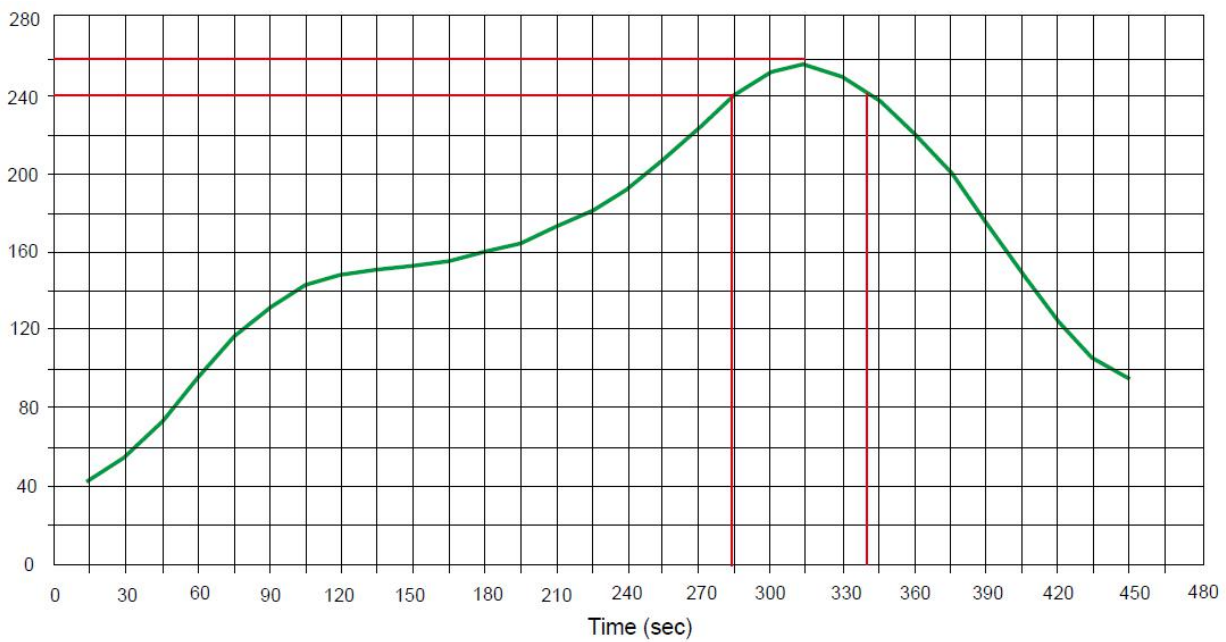
Non-Repetitive Peak Pulse Power vs. Pulse Time



Insertion Loss S21

● Solder Reflow Recommendation

Peak Temp=257°C, Ramp Rate=0.802deg. °C/sec



● Package Information

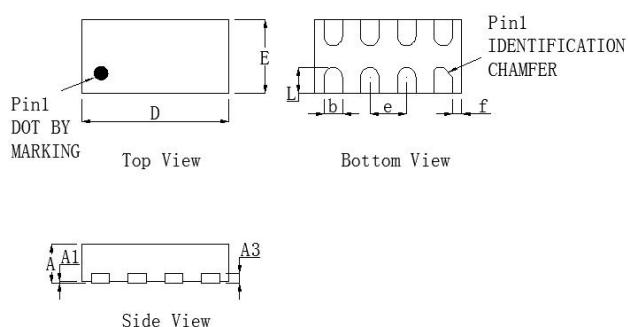
Ordering Information

Device	Package	Marking	Qty per Reel	Reel Size
TQELN8122V5	DFN2010-8L	2R2P	3000	7 Inch

Mechanical Data

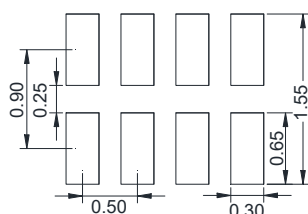
Case:DFN2010-8L

Case Material: Molded Plastic. UL Flammability



DIM	Millimeters		
	Min	Nom	Max
A	0.45	-	0.5
A1	0.00	-	0.05
A3	0.125 REF		
D	1.95	2.00	2.05
E	0.95	1.00	1.05
b	0.20	0.25	0.30
L	0.30	0.35	0.40
e	0.50 BSC		
f	0.125 REF		

Recommended Pad outline



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